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**SM2260**

**SSD Flash Controller**

SSD MP Pretest Light Switch

Confidential

Version : 1.0

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# Update History

|  |  |  |  |
| --- | --- | --- | --- |
| Date | Version | Description | Editor |
| O1023 | 1.0.0 | First version | Maxgale |

# Introduction

This pretest light switch is an optional function which can help to change the drive’s setting in the pretest flow, which includes DRAM Driving Strength, DRAM ODT, DRAM DLL offset after chaining, Flash Driving Strength, Flash ODT, and Flash DLL offset tuning after training. The application’s functionality and operation flow will be introduced by this document.

# Quick Start

Step 1: Under MPTool folder, open “LightSwitch\_SM2260.exe” and select the “Pretest” under “Option”.

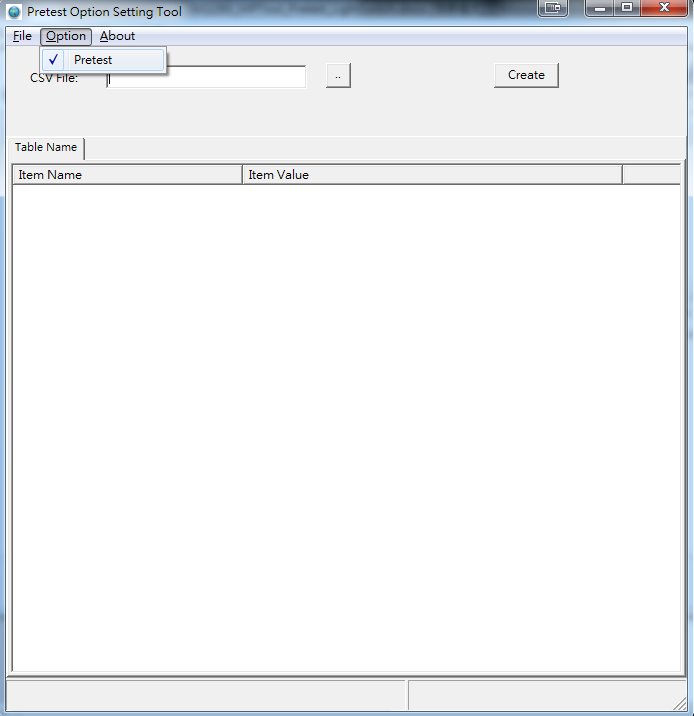


Figure 1

Step 2: Load “SM2260\_PretestSet\_LightSwitch\_description\_O1029.csv” under “PretestOption” folder.



Figure 2

Step 3: Set the desired the Pretest Light Switch setting and create .bin and .csv file under “PretestOption” folder.



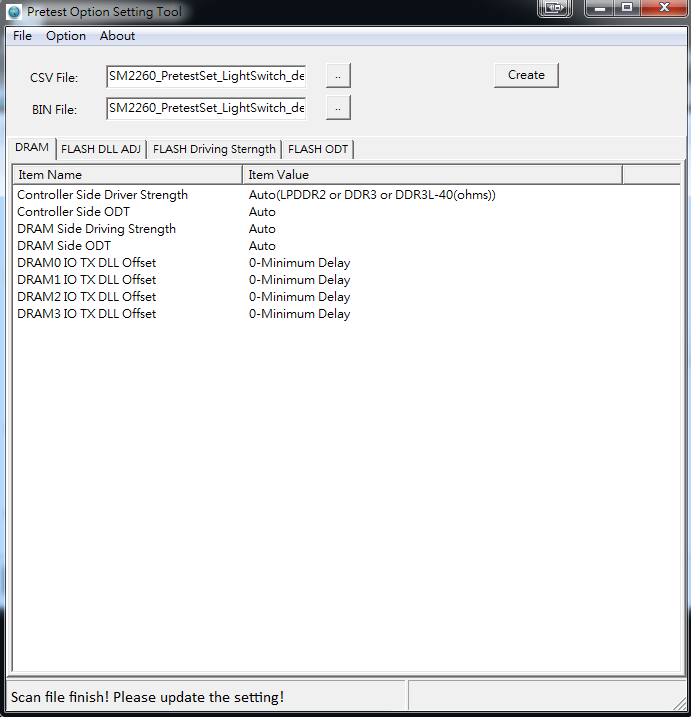
Figure 3

Step 4: Put the newest .bin file into “firmware” folder. Then open MPTool and enter “Pretest Set” function and in the “Other Pretest Setting” select the above .bin file in “firmware” folder and press “Update” to check or adjust the setting in Step3.



Figure 4

Step 5: Press “Create” after check or adjust the corresponding pretest setting. Then the new .bin file will both update in “firmware” folder and create a new backup in “PretestOption” folder.

Figure 5

Step 6: Press “Save” in the “Pretest Setting” and perform the open card.

# Functionality

**DRAM**

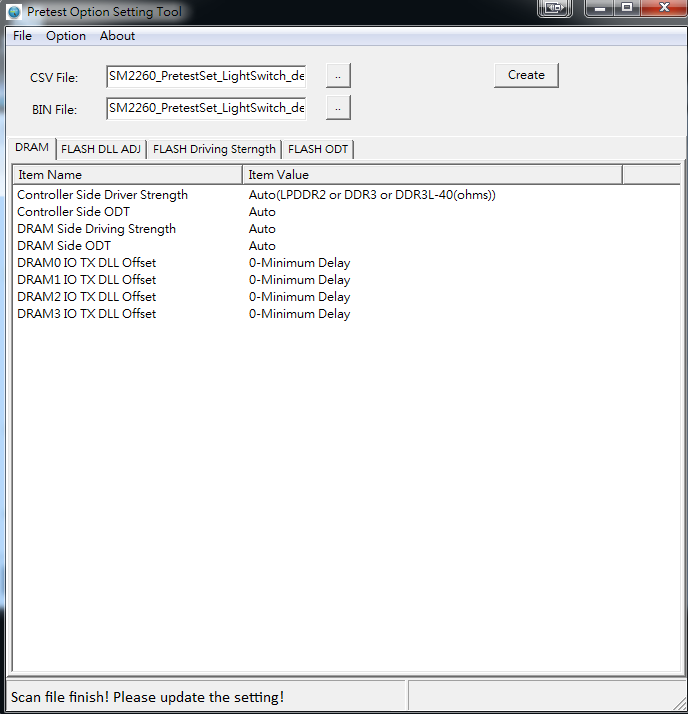
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Figure 6

**DRAM, Controller Side Driving Strength/ODT**: In the MPTool→Preteset Set→Other Pretest Setting→Update, Select DRAM tab, set the corresponding Controller Side Driving Strength/ODT value. After pretest flow(and reboot), we can check the setting by EzTools by selecting option “DRAM RW” and accessing the Addr (H): (0x)50801184 to check the value [Bit3-Bit0] as Table 1 for Controller Side Driving Strength and [Bit7-Bit4] as Table 2 for Controller Side ODT.

**Table 1 DRAM Controller Side Driving Strength**

|  |  |  |
| --- | --- | --- |
| Value | DDR3 | LPDDR2 |
| 0x5 |  | 80 ohms |
| 0x7 |  | 60 ohms |
| 0x9 |  | 48 ohms |
| 0xB | 40 ohms | 40 ohms |
| 0xD | 30 ohms | 30 ohms |

Currently supports DDR3 and LPDDR2.

**Table 2 DRAM, Controller Side ODT**

|  |  |
| --- | --- |
| Value | DDR3 |
| 0x1 | 120 ohms |
| 0x5 | 60 ohms |
| 0x8 | 40 ohms |

Currently supports DDR3.

**DRAM, DRAM Side Driving Strength**: In the MPTool→Preteset Set→Other Pretest Setting→Update, Select DRAM tab, set the corresponding DRAM Side Driving Strength value. After pretest flow(and reboot), we can check the DDR3/DDR3L’s setting by EzTools’s “DRAM RW” function and accessing the Addr (H): (0x)50801044 to check the value in the Bit1 as Table 3, for example, when selecting DDR3/DDR3L RZQ7, Addr (H): 50801044 Bit1=1. For LPDDR2, we can check by accessing the Addr (H): 5080104C, and check the value in [Bit2:Bit1:Bit0] as Table 3..

**Table 3 DRAM, DRAM Side Driving Strength**

|  |  |  |
| --- | --- | --- |
| Value | DDR3 | LPDDR2 |
| 0x7 |  | 120 ohms |
| 0x6 |  | 80 ohms |
| 0x4 |  | 60 ohms |
| 0x3 |  | 48 ohms |
| 0x2 |  | 40 ohms |
| 0x1 | RZQ/7 | 34 ohms |
| 0x0 | RZQ/6 |  |

Currently supports DDR3/DDR3L and LPDDR2.

**DRAM, DRAM Side ODT**: In the MPTool→Preteset Set→Other Pretest Setting→Update, Select DRAM tab, set the corresponding DRAM Side ODT value. After pretest flow(and reboot), we can check by accessing the Addr (H): (0x)50801044 by EzTools’s “DRAM RW” function to check the value in [Bit9:Bit6:Bit2] as Tabl3 4.

**Table 4 DRAM, DRAM Side ODT**:

|  |  |
| --- | --- |
| Value | DDR3 |
| 0b100 | RZQ/12 |
| 0b101 | RZQ/8 |
| 0b011 | RZQ/6 |
| 0b001 | RZQ/4 |
| 0b010 | RZQ/2 |
| 0b000 | Disabled |

Currently supports DDR3.

**DRAM, DRAMn IO TX DLL:** In the MPTool→Preteset Set→Other Pretest Setting→Update, Select DRAM tab, set the corresponding DRAMn IO TX DLL Offset value. After pretest flow(and reboot), we can check by accessing the Addr (H): (0x)508011CC/DRAM0, (0x)5080120C/DRAM1(if existed), (0x)5080124C/DRAM2(if existed), and (0x)5080128C/DRAM3(if existed) by EzTools’s “DRAM RW” function to check the value in [Bit11:Bit10:Bit9] as Table 5.

**Table 5 DRAM, DRAMn IO TX DLL**

|  |  |
| --- | --- |
| Value | DDR3/LPDDR2 |
| 0b000 | 0 (Minimum Delay) |
| 0b001 | 1 |
| 0b010 | 2 |
| 0b011 | 3 |
| 0b100 | 4 |
| 0b101 | 5 |
| 0b110 | 6 |
| 0b111 | 7 (Maximum Delay) |

**FLASH DLL ADJ:** flash channel TX/RX DLL offset tuning after training. In the MPTool→Preteset Set→Other Pretest Setting→Update, Select FLAH DLL ADJ tab, and set the corresponding flash channel’s TX/RX DLL ADJ offset value. After pretest flow(and reboot), we can check by accessing the Addr (H): (0x)5110011F/Channel0, (0x)5111011F/Channel1, (0x)5112011F/Channel2, (0x)5113011F/Channel3, (0x)5114011F/Channel4, (0x)5115011F/Channel5, (0x)5116011F/Channel6, (0x)5117011F/Channel7 by EzTools’s “DRAM RW” function to check the corresponding TX/RX DLL ADJ offset value in [Bit7-Bit4]/[Bit3-Bit9] as Table 6.

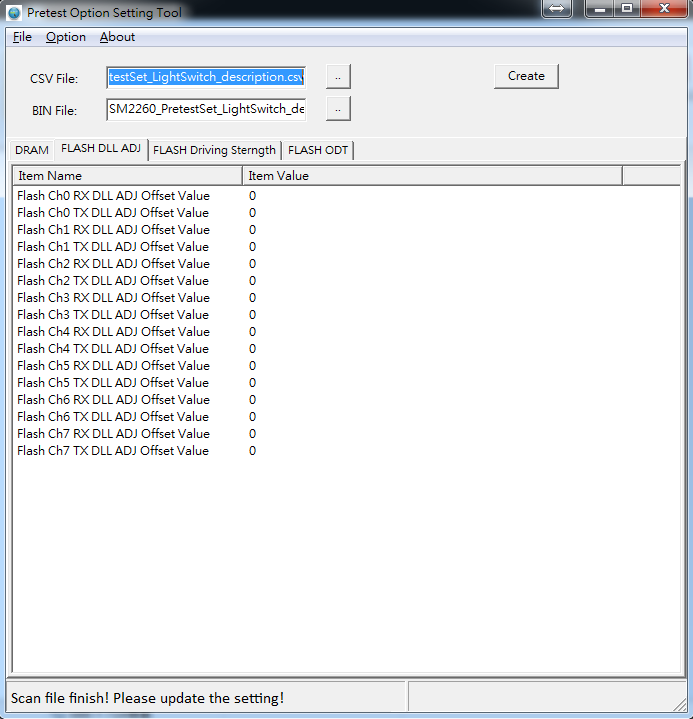


Figure 7

**Table 6**

|  |  |
| --- | --- |
| Value | DLL Offset Tuning Value |
| 0xF | -7 |
| 0xE | -6 |
| 0xD | -5 |
| 0xC | -4 |
| 0xB | -3 |
| 0xA | -2 |
| 0x9 | -1(DQS\_90 shift forward) |
| 0x8 | 0 (no ADJ tuning) |
| 0x1 | 1(DQS\_90 shift backward) |
| 0x2 | 2 |
| 0x3 | 3 |
| 0x4 | 4 |
| 0x5 | 5 |
| 0x6 | 6 |
| 0x7 | 7 |
|  |  |

**FLASH Driving Strength:** Pull Up and Pull Down driving strength of each flash channel’s WE/RE/CLE/AES/DQ/DQS. In the MPTool→Preteset Set→Other Pretest Setting→Update, Select FLAH Driving Strength tab, we first Enable the desired channel and set the corresponding pull up/pull down WE/RE/CLE/AES/DQ/DQS driving strength value. If disable, pretest flow will use the hardware default value. After pretest flow(and reboot), we can check the value by accessing the corresponding Addr(H) as Table 7 by EzTools’s DRAM RW function.

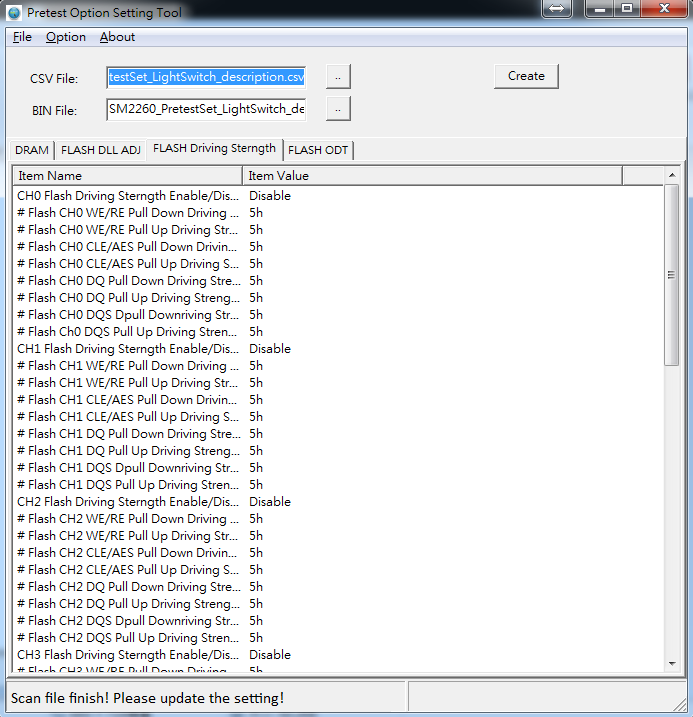


Figure 8

**Table 7**

|  |  |  |
| --- | --- | --- |
| **Flash CH** | **Addr(H)** | **WE/RE/CLE/AES/DQ/DQS**  **driving strength** |
| Flash Channel 0 | (0x)50000090 | WE/RE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)50000092 | CLE/ALE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)50000094 | DQ  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)50000096 | DQS  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| Flash Channel 1 | (0x)50000098 | WE/RE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)5000009A | CLE/ALE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)5000009C | DQ  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)5000009E | DQS  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| Flash Channel 2 | (0x)500000A0 | WE/RE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000A2 | CLE/ALE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000A4 | DQ  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000A6 | DQS  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| Flash Channel 3 | (0x)500000A8 | WE/RE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000AA | CLE/ALE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000AC | DQ  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000AE | DQS  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| Flash Channel 4 | (0x)500000B0 | WE/RE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000B2 | CLE/ALE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000B4 | DQ  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000B6 | DQS  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| Flash Channel 5 | (0x)500000B8 | WE/RE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000BA | CLE/ALE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000BC | DQ  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000BE | DQS  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| Flash Channel 6 | (0x)500000C0 | WE/RE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000C2 | CLE/ALE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000C4 | DQ  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000C6 | DQS  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| Flash Channel 7 | (0x)500000C8 | WE/RE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000CA | CLE/ALE  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000CC | DQ  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |
| (0x)500000CE | DQS  Pull Up[Bit7-Bit4]/Pull Down[Bit3-Bit0] |

**FLASH ODT:** DQ and DQS ODT setting of each flash channel. In the MPTool→Preteset Set→Other Pretest Setting→Update, Select FLAH ODT tab, we first Enable the desired channel and set the corresponding DQ and DQS ODT value. If disable, pretest flow will use the hardware default value. After pretest flow(and reboot), we can check the value by accessing the corresponding Addr(H) as Table 8 by EzTools’s DRAM RW function.

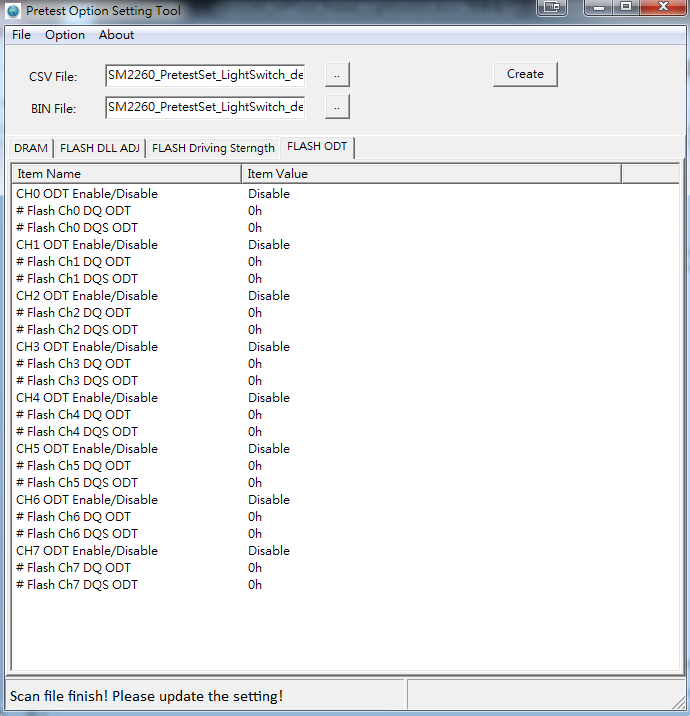


Figure 9

**Table 8**

|  |  |  |
| --- | --- | --- |
| **Flash CH** | **Addr(H)** | **WE/RE/CLE/AES/DQ/DQS**  **driving strength** |
| Flash Channel 0 | (0x)51000040 | DQ ODT[Bit3-Bit0] |
| (0x)51000041 | DQS ODT[Bit3-Bit0] |
| Flash Channel 1 | (0x)51000044 | DQ ODT[Bit3-Bit0] |
| (0x)51000045 | DQS ODT[Bit3-Bit0] |
| Flash Channel 2 | (0x)51000048 | DQ ODT[Bit3-Bit0] |
| (0x)51000049 | DQS ODT[Bit3-Bit0] |
| Flash Channel 3 | (0x)5100004C | DQ ODT[Bit3-Bit0] |
| (0x)5100004D | DQS ODT[Bit3-Bit0] |
| Flash Channel 4 | (0x)51000050 | DQ ODT[Bit3-Bit0] |
| (0x)51000051 | DQS ODT[Bit3-Bit0] |
| Flash Channel 5 | (0x)51000054 | DQ ODT[Bit3-Bit0] |
| (0x)51000055 | DQS ODT[Bit3-Bit0] |
| Flash Channel 6 | (0x)51000058 | DQ ODT[Bit3-Bit0] |
| (0x)51000059 | DQS ODT[Bit3-Bit0] |
| Flash Channel 7 | (0x)5100005C | DQ ODT[Bit3-Bit0] |
| (0x)5100005D | DQS ODT[Bit3-Bit0] |